IN THE CLAIMS

Please add the following claims:

23. (New) An apparatus comprising:

a memory ordering unit to schedule loads comprising a load buffer to store a first instruction and a prior load operation

scheduled prior to said first instruction;

a cache controller comprising a cache controller buffer to store load data addressed by said prior load operation, said first instruction to be dispatched from said load buffer to said cache controller after said load data is stored in said cache controller buffer and globally observed;

a hit/miss detector to select said cache controller buffer if said prior load operation corresponds to a cache miss or uncacheable request.

24. (New) The apparatus of claim 23 wherein instructions following said first instruction in program order are prevented from being dispatched to said cache controller until said first instruction is accepted by said cache controller.

25. (New) The apparatus of claim 23 wherein after said load data is globally observed, said load data is to be read to a register and de-allocated from said cache controller buffers.

26. (New) The apparatus of claim 23 further comprising a control register, said control register comprising a first control bit and a second control bit.

27. (New) The apparatus of claim 26 wherein said first control bit enables pre-serialization of load operations scheduled prior to said first instruction.

28. (New) The apparatus of claim 27 wherein said second control bit enables post-serialization of load operations scheduled after said first instruction.

29. (New) The apparatus of claim 28 wherein if said pre-serialization and said post-serialization are enabled, all load operations scheduled after said first instruction are prevented from being dispatched to said cache controller until all load operations issued prior to said first instruction are globally observed within said cache controller buffer.

30. (New) A system comprising:

a memory unit;

a processor, said processor comprising a load buffer to store a first instruction and a cache controller to block said first instruction until load data fetched from said memory unit is globally observed;

a bus agent to snoop said load data;

a bus to couple said memory unit and said bus agent to said processor.

31. (New) The system of claim 30 wherein said processor further comprises a control register to enable control of pre-serialization and post-serialization of load operations.

32. (New) The system of claim 30 wherein said memory unit comprises a first and second load operation separated in program order by said first instruction to be fetched by said processor.

33. (New) The system of claim 32 wherein said second load operation does not appear on said bus until target data of said first load operation is loaded into said processor and subsequently observed by said bus agent.

34. (New) The system of claim 31 wherein said memory unit comprises a first plurality of load operations and a second plurality of load operations separated in program order by said first instruction.

35. (New) The system of claim 34 wherein said first plurality of load operations are serialized with respect to said first instruction and said second plurality are serialized with respect to said first instruction.

36. (New) The system of claim 34 wherein said first plurality of load operations appear on said bus before said second plurality of load operations.

37. (New) The system of claim 34 wherein target data of each of said first plurality of load operations is loaded into said processor and subsequently observed by said bus agent before said second plurality of load operations appear on said bus.

38. (New) The system of claim 37 wherein said first instruction is a load fence (LFENCE) instruction.